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An Efficient VLSI Implementation of OFDM based on Multiplier Less FFT & IFFT

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Abstract: Orthogonal Frequency Division Multiplexing (OFDM) is a multi-carrier system where data bits are encoded to multiple subcarriers, while being sent simultaneously. OFDM is implemented by using the combination of FFT and IFFT. The Eight point DIT-FFT & DIF IFFT architecture is implemented as a Multiplier less architecture. The eight point DIT-FFT & DIF IFFT architecture consist of two points, four points, Eight Point as Stages. The OFDM architecture was implemented based on proposed Multiplier less FFT and IFFT Block. Fast Fourier Transform is one of the important algorithms in Digital signal processing (DSP).. In this proposed method the unity gain FFTs and IFFTs without compensation circuits is implemented by using shift and add method. It reduces the amount of hardware resources of the architecture with high accuracy in calculation. This proposed method can be applied to different sizes of FFT for various designs. This approach can be Implemented using Verilog HDL and Simulated by Modelsim 6.4 c. Finally it is synthesized by Xilinx tool and Implemented in FPGA Spartan 3 XC3S 200 TQ-144.

Keywords: OFDM, multiplier less FFT, multiplier less IFFT.

I. INTRODUCTION

Digital signal processing (DSP) world, there is often a need to convert signals between time and frequency domains. OFDM is a multi-carrier system where data bits are encoded to multiple sub-carriers. Unlike single carrier systems, all the frequencies are sent simultaneously in time. OFDM offers several advantages over single carrier system like better multi-path effect immunity, simpler channel equalization and relaxed timing acquisition constraints. But it is more susceptible to local frequency offset and radio front-end non - linearities. The frequencies used in OFDM system are orthogonal. Neighboring frequencies with overlapping spectrum can therefore be used. The OFDM is therefore able to provide higher data rate for the same BW OFDM is fast gaining popularity in broadband standards and high speed wireless LAN. For this reason, the fast Fourier transform (FFT) has become one of the most important algorithms in the field. In order to calculate the FFT efficiently, various hardware architectures have been proposed. When high performance is required, feedback and feed forward, hardware FFT architectures are attractive options, as they offer high throughput capabilities. Single-delay feedback (SDF) FFT architectures consist of a series of stages that process one sample per clock cycle. Each stage contains a butterfly and a rotator. The butterfly calculates additions, and the rotator carries out rotations in the complex plane by given rotation angles, called twiddle factors. Compared with the additions of the butterfly, rotations are more costly operations. For this reason, different approaches to implement rotators have been proposed in the past. The most straightforward approach is to use a complex multiplier, which consists of four real multipliers and two adders. In addition, it requires a memory to store the twiddle factors. Another option is to implement the rotators as shift-and-add operations.

Following this idea, the CORDIC algorithm breaks down the rotation angle into several successively smaller angles and rotates each of them with a fixed shift-and-add network. Another alternative is to use multiplier-based shift-and-add rotators. By using techniques, such as multiple constant multiplications, these rotators carry out the rotation by reducing the complex multiplier to shift-and-add operations. Among all these alternatives, multiplier-based shift-and-add rotators, are the most efficient option for small set point SDF FFT architecture, using n = 6 stages. Internal structure of an SDF stage. Of twiddle factors, whereas the CORDIC-based rotators [2] are the best alternative for large ones. However, CORDIC-based approaches and some multiplier-based shift-and-add rotators, scale the output by a scaling factor $R \neq 1$. This scaling allows for more accurate and hardware-efficient rotations. In order to achieve unity gain, previous works have compensated the scaling factor by adding a scaling stage to the rotator. However, this increases the usage of hardware resources. In this brief, we present the novel multiplier less unity-gain SDF FFTs. They are obtained by designing the rotators in all FFT stages simultaneously. So that the output of the FFT has unity gain. Thus, the proposed approach neither requires the use of costly unity-gain rotators, nor circuits to compensate the scaling. This reduces the complexity of the FFT rotators and guarantees unity gain for the FFT.

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II.RELATED WORK

The existing method presents an approach for improving the accuracy of rotations implemented by complex multipliers, based on scaling the complex coefficients that define these rotations. A method for obtaining the optimum coefficients that lead to the lowest error is proposed. It analyzes two different situations where the optimization method can be applied: rotations that can be optimized independently and sets of rotations that require the same scaling. These cases appear in important signal processing algorithms such as the discrete cosine transform and the fast Fourier transform (FFT).Unity-gain FFTs by using either complex multipliers[1].This approach can be used to get more accurate rotations without increasing the coefficient word length but it's got less accurate and Rotation error is high .
Orthogonal Frequency Division Multiplexing (OFDM) is a multi-carrier system where data bits are encoded to multiple sub-carriers, while being sent simultaneously. This results in the optimal usage of bandwidth. A set of orthogonal sub-carriers together forms an OFDM symbol. To avoid ISI due to multi-path, successive OFDM symbols are separated by guard band.[3].

III. MUTIPLIER LESS FFT ARCHITECTURE

Here the multiplier less unity-gain SDF FFTs was presented. They are obtained by designing the rotators in all FFT stages simultaneously, so that the output of FFT has unity gain. Thus, the proposed approach neither requires the use of costly unity-gain rotators, nor circuits to compensate the scaling. This reduces the complexity of the FFT rotators and guarantees unity gain for the FFT. The Design of an OFDM architecture based on our proposed Multiplier less FFT and IFFT Block. Mathematically modulating a waveform and adding it is equivalent to taking an IFFT. This is because the time domain representation of OFDM is made up of different orthogonal sinusoidal signals which are nothing but inverse Fourier transform. The block diagram of digital OFDM system is shown in Figure.

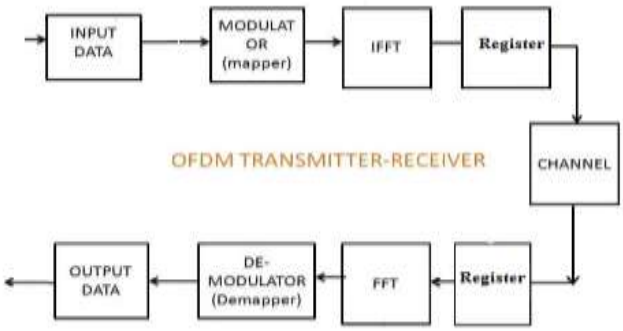

Fig. No.3 (a)Block Diagram of OFDM

We have to implement the OFDM block by block and finally interconnect all of them together to form complete OFDM circuit.
Inverse Fast Fourier Transform (IFFT) Initially carrier bank generating a set of subcarriers was necessary for OFDM in conventional or analogue approach. Each subcarrier was modulated with a constellation decided by bit combination, but this approach made system bulky and costlier. So to make system digital, simple, cheap, and efficient IFFT is being used. A stepwise implementation of butterfly diagram is done in this algorithm. Radix-2 Decimation-in-time (DIF) IFFT is implemented in this algorithm. Different procedures and operations are done to achieve this. In Fig. 3(b). the basic butterfly unit for the radix-2 IFFT algorithm is shown.

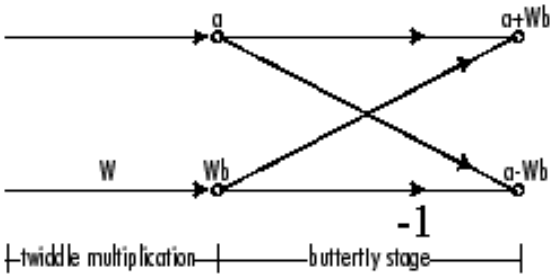

Fig. 3(b): Decimation-In-Time IFFT

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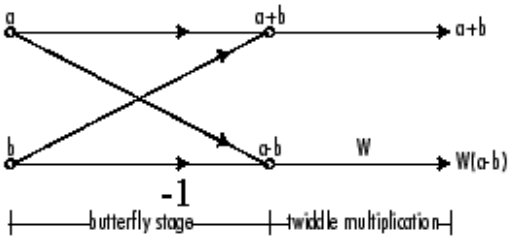

Fig. 3(b): Decimation-In-Frequency FFT

FFT and Demodulator For FFT inverse process of IFFT and for Demodulation inverse process of Modulation is used. In this design at FFT, if its output 2.999 then FFT shows it as a 2 instead of 3. Care of this type of problems is taken by demodulator; it gives output as 3 for input 2 or3.

IV. IMPLEMENTATION OF OFDM

OFDM is a combination of modulation and multiplexing. Multiplexing generally refers to independent signals, those produced by different sources. In OFDM the signal itself is first split into independent channels, modulated by data and then re-multiplexed to create the OFDM carrier. OFDM is a special case of Frequency Division Multiplex (FDM). Since the OFDM signal is in time domain, IFFT is the appropriate choice to use in the transmitter, which can be thought of as converting frequency domain samples to time domain samples. Fig. 2 illustrates how the use of IFFT in the transmitter eliminates the need for separate sinusoidal converters. IFFT and FFT blocks in the transmitter are interchangeable as long as their duals are used in receiver.

V. SHIFT AND ADD METHOD

The multiplier less IFFT and FFT blocks are implemented by using the shift and add method instead of using the complex rotators. Then by combining the IFFT and FFT blocks OFDM is implemented. The shift and add algorithm is followed.

Step 1: initialize the data segment.
Step 2: Get the first number
Step 3: Get the second number
Step 4: Initialize the count =04
Step 5: Number 1= number1'2
Step 6: Shift multiplier left along with carry
Step 7: Check for carry if present go to step 8 else go to step9.
Step 8: Number 1=number1+ shifted number 2
Step 9: Decrement the counter
Step 10: if not zero go to step 5
Step 11: Display the result.

V. RESULT AND OUTPUT

In this proposed multiplier less OFDM implementation architecture number of LUTs are reduced and total delay is considerably reduced.

Table.5a.Comparision

METHOD NAME	AREA				DELAY		
	LUT	SLICES	GATE	IOB	OVER ALL	GATE	PATH
MULTIPLIERS BASED OFDM	2890	1474	30659	512	31.858ns	20.369ns	11.489ns
MULTI PLIER LESS OFDM	1698	990	18478	512	26.801ns	13.561ns	13.240ns

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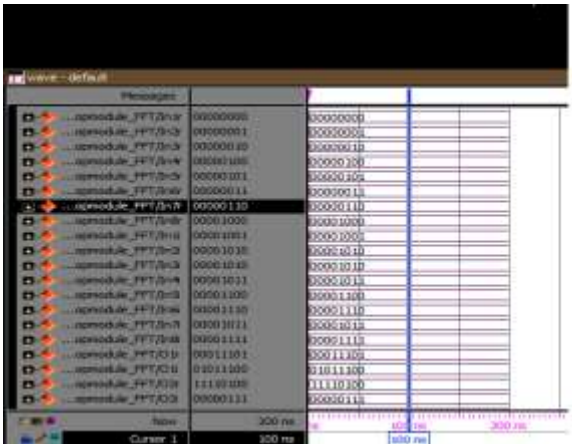

Fig.5a.Output of FFT

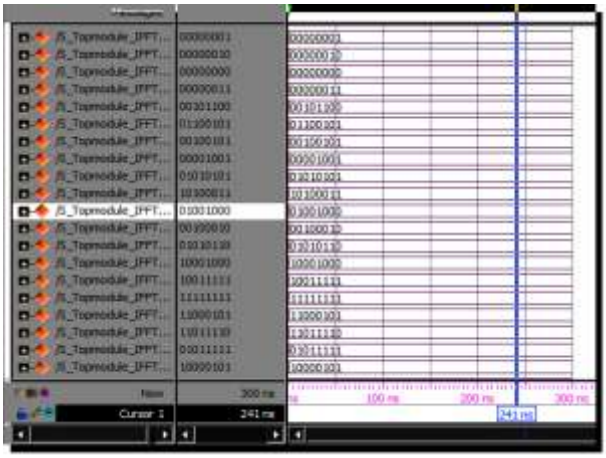

Fig.5b.ouput of IFFT

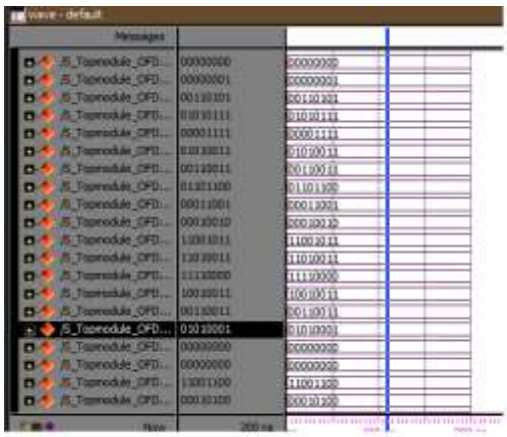

Fig.5c.output of OFDM

VI. CONCLUSION

This technique shows how to design multiplier less unity-gain SDF OFDM architectures. The proposed architectures are not only multiplier less and achieve Less area and Delay, but also require the smallest number of adders among current SDF OFDM. The proposed architectures achieve good figures of merit in terms of clock frequency, area. The 8 Point OFDM implemented by Verilog HDL and Simulated in Model sim 6.4 c and Synthesized in Xilinx 9.1 tool.

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